# Dynamic Hysteresis Band Control of the Buck Converter With Fast Transient Response

Kelvin Ka-Sing Leung, Student Member, IEEE, and Henry Shu-Hung Chung, Senior Member, IEEE

*Abstract*—A dynamic hysteresis control of the buck converter for achieving high slew-rate response to disturbances is proposed. The hysteresis band is derived from the output capacitor current that predicts the output voltage magnitude after a hypothesized switching action. Four switching criteria are formulated to dictate the state of the main switch. The output voltage can revert to the steady state in two switching actions after a large-signal disturbance. The technique is verified with the experimental results of a 50 W buck converter.

*Index Terms*—Boundary control, DC–DC power conversion, large-signal stability, state trajectory prediction.

## I. INTRODUCTION

UCH research work has been recently focused on the control schemes to improve the large-signal dynamics in dc/dc conversion. Concept of current control [1]-[3] combines the slow-varying voltage loop with the fast-varying current loop to dictate the state of the main switch. A best performance can be obtained when the current reference and the inductor current are closely related [4]. Recently,  $V^2$  control provides fast loop responses [5], [6]. The proposed architecture uses the equivalent series resistance (ESR) of the output capacitor for obtaining information on the current. Thus, the ESR becomes a critical factor that considerably affects the converter performance, since it affects the accuracy of the measured current. Another one is the hysteresis control [7], [8] that the controller turns the switch on when the output is below the hysteresis band, and vice versa. However, during the startup and load disturbance, the energy stored in the inductor will continuously boost the output, even if the controller turns the main switch off. Eventually, the settling time will be lengthened.

Another approach is based on state-trajectory control [9]–[11] that the converter can achieve steady-state operation for a step change in input voltage or output current in one on/off control, but the control requires either sophisticated digital processor or analog computation. This paper proposes an enhancement of the above methods. The technique requires simple implementation and is based on state-trajectory-prediction (STP). It can enhance the transient response of the buck converter with hysteresis control. The output can revert to the steady state in two switching actions after a large-signal

The authors are with the Department of Electronic Engineering, City Univer-

Digital Object Identifier 10.1109/TCSII.2005.850411



Fig. 1. Buck converter.



Fig. 2. Typical waveforms of  $v_o$  and  $i_C$ .

disturbance. The theoretical predictions have been verified experimentally. Finally, effects of the ESR of the output capacitor on the converter performance will be presented.

## II. PRINCIPLES OF OPERATION

Fig. 1 shows the circuit schematic of the buck converter. When the switch S is on

$$\frac{di_L}{dt} = \frac{1}{L}(v_i - v_o) \quad \text{and} \quad \frac{dv_o}{dt} = \frac{dv_C}{dt} = \frac{1}{C}i_C.$$
(1)

When S is off and D is on

$$\frac{di_L}{dt} = -\frac{1}{L}v_o \quad \text{and} \quad \frac{dv_o}{dt} = \frac{dv_C}{dt} = \frac{1}{C}i_C.$$
 (2)

When S and D are off

$$\frac{di_L}{dt} = 0 \quad \text{and} \quad \frac{dv_o}{dt} = \frac{dv_C}{dt} = \frac{1}{C}i_C.$$
 (3)

If the output ripple voltage is much smaller than the average output voltage at the steady state, the output current  $i_o$  is relatively constant. Since  $i_L = i_C + i_o$ , the change of  $i_L$ ,  $\Delta i_L$ , equals the change of  $i_C$ ,  $\Delta i_C$ . Fig. 2 shows the typical waveforms of  $v_o$  and  $i_C$ .  $v_o$  varies between a maximum value of  $v_{o,\text{max}}$  and a minimum value of  $v_{o,\text{min}}$ . The state of S is determined by predicting the area under  $i_C$  with a hypothesized switching action till  $i_C = 0$  and comparing the area with a fixed ratio of the output error at that instant.

#### A. Criteria for Switching on S

As shown in Fig. 2, S is originally in the off state and is switched on at the hypothesized time instant  $t_1$ . The objective is

Manuscript received November 21, 2002; revised November 15, 2004. This work was supported by the City University of Hong Kong under Project 7001595. This paper was recommended by Associate Editor I. A. Hiskens.

sity of Hong Kong, Hong Kong (e-mail: eeshc@cityu.edu.hk).

to determine  $t_1$ , so that  $v_o$  will be equal to  $v_{o,\min}$  at  $t_2$  (at which  $i_C = 0$ ). The shaded area  $A_1$  under  $i_C$  is integrated from  $t_1$  to  $t_2$ . Thus

$$\Delta v_{o,1} = v_o(t_1) - v_{o,\min} = -\frac{1}{C} \int_{t_1}^{t_2} i_C \, dt. \tag{4}$$

If  $A_1$  is approximated by a triangle, it can be shown that

$$\int_{t_1}^{t_2} i_C dt \cong -\frac{1}{2} \frac{L i_C^2(t_1)}{[v_i(t_1) - v_o(t_1)]}.$$
(5)

In order to ensure that  $v_o$  will not go below  $v_{o,\min}$ , S should be switched on when

$$v_{o}(t_{1}) \leq v_{o,\min} + \frac{L}{2C[v_{i}(t_{1}) - v_{o}(t_{1})]} i_{C}^{2}(t_{1})$$
(6)  
=  $v_{o,\min} + K_{1}(v_{i}, v_{o}) i_{C}^{2}(t_{1})$  and  $i_{C}(t_{1}) < 0.$  (7)

# B. Criteria for Switching off S

As shown in Fig. 2, S is originally in the on state and is switched off at the hypothesized time instant  $t_3$ . The objective is to determine  $t_3$ , so that  $v_o$  will be equal to  $v_{o,\max}$  at  $t_4$  (at which  $i_C = 0$ ). The shaded area  $A_2$  under  $i_C$  is integrated from  $t_3$  to  $t_4$ . Thus

$$\Delta v_{o,2} = v_{o,\max} - v_o(t_3) = \frac{1}{C} \int_{t_3}^{t_4} i_C \, dt. \tag{8}$$

Again,  $A_2$  is approximated by a triangle. It can be shown that

$$\int_{t_3}^{t_4} i_C dt \cong \frac{1}{2} \frac{Li_C^2(t_3)}{v_o(t_3)}.$$
(9)

In order to ensure that  $v_o$  will not go above  $v_{o,\max}$ , S should be switched off when

$$v_o(t_3) \ge v_{o,\max} - \frac{L}{2Cv_o(t_3)} i_C^2(t_3)$$
 (10)

$$= v_{o,\max} - K_2(v_o) i_C^2(t_3)$$
 and  $i_C(t_3) > 0.$  (11)

If  $K_1$  and  $K_2$  are zero, the control is same as an ordinary hysteresis control. The time-varying error terms in (6) and (10) (i.e., the second term) affect the output ripple and improve the transient responses, as compared with the ordinary hysteresis control. For the sake of simplicity,  $v_i$  and  $v_o$  in (6) and (10) are taken to be their nominal values. Thus,  $K_1$  and  $K_2$  are constants. The criteria of (6), (7), (10), and (11) are applied for both steadystate operation and large-signal disturbances. Fig. 3 shows the block diagram of the control.

### **III. EXPERIMENTAL VERIFICATIONS**

A 50-W 24 V/5 V prototype has been built. The component values are:  $L = 100 \ \mu$ H,  $C = 470 \ \mu$ F,  $r_L = 250 \ m\Omega$ ,  $r_C = 20 \ m\Omega$ ,  $v_{o,\min} = 4.975 \ V$ , and  $v_{o,\max} = 5.025 \ V$ .  $v_o$  is regulated at 5 V. The theoretical state-plane trajectories



Fig. 3. Block diagram of the control technique.



Fig. 4. Theoretical state-plane trajectories of the buck converter operating at the rated power from different initial conditions. (a) Without STP. (b) With STP.

operating at the rated load under five different load disturbances without and with the STP are shown in Fig. 4(a) and (b), respectively. They show the changes of  $i_L$  (i.e.,  $\hat{i}_L$ ) and  $v_o$  (i.e.,  $\hat{v}_o$ ) during the transient period. The origin (0, 0) represents the steady-state operating point of  $v_o = 5$  V and  $i_L = 10$  A.

TABLE I COMPARISONS OF CONVERTER TRANSIENT RESPONSES WITH AND WITHOUT STP

Testing condition		1		2		3		4		5
<i>i</i> <sub><i>L</i></sub> (0 <sup>-</sup> ) (A)	0.1		2		4		14		16	
	Without	With STP								
	STP		STP		STP		STP		STP	
Settling time (µs)	248.7	102.4	182.7	79.3	135.4	53.3	77.0	77.0	144.1	118.1
% output overshoot	5.7	0.0	3.7	0.0	1.8	0.0	2.4	2.4	5.8	5.8
Max. inductor current (A)	16.8	14.7	15.5	13.9	14.2	13.0	14.0	14.0	16.0	16.0



Fig. 5. Startup transients. [ $v_o$ : output voltage (1 V/div),  $i_i$ : input current(10 A/div),  $i_o$ : load current (10 A/div),  $v_g$ : gate drive signal(10 V/div)]. (a) Without STP. (b) With STP.

The initial deviations from the steady state operating point (i.e., the testing conditions) are labeled from "1" to "5" in the figures. The initial inductor currents prior load changes [i.e.,  $i_L(0^-)$ ], the settling time, the percentage output overshoots are tabulated in Table I. The settling time is defined as the time taken that  $v_o$  falls into  $\pm 1\%$  tolerance bands – the dash lines shown in the figures. It can be seen that the transient



Fig. 6. Transient responses when  $i_o$  is changed from 1 A (5 W) to 10 A (50 W). [ $v_o$ : output voltage (200 mV/div),  $i_C$ : capacitor current(10 A/div),  $i_o$ : load current (10 A/div),  $v_g$ : gate drive signal(10 V/div)] (a) Without STP. (b) With STP.

performances are improved with the STP, particularly when the output load is increased.

Fig. 5 shows the startup transients of  $v_o$ , the input current  $i_i$ ,  $i_o$ , and the gate drive signal  $v_g$  without and with the STP. The settling time of the output transient without STP is 650  $\mu$ s, whilst the one with STP is 350  $\mu$ s. As expected, the ordinary hysteresis control turns off the main switch when  $v_o$ 



Fig. 7. Transient responses when  $i_o$  is changed from 5 A (25 W) to 0.4 A (2 W). [ $v_o$ : output voltage (200 mV/div),  $i_C$ : capacitor current(5 A/div),  $i_o$ : load current (5 A/div),  $v_a$ : gate drive signal(10 V/div)].



Fig. 8. State-plane trajectories of the converters when  $i_L$  is changed from 0.1 A to 10 A with the ESR of the output capacitor varying from 0  $\Omega$  to 100 m $\Omega$ .

is higher than the hysteresis band. The stored energy in the inductor will further boost the output after the main switch is off. The output overshoot and settling time are thus increased. The output profile is much improved with the STP. However, as  $i_o$  is not in the steady state during the startup,  $\Delta i_L$  is different from  $\Delta i_C$ . There are discrepancies in predicting the output. As circled in Fig. 5(b), two extra switching actions are introduced, but it does not affect the overall performance. Fig. 6 shows the waveforms when  $i_o$  is increased suddenly from 1 A (5 W) to 10 A (50 W). The settling time of the transients without STP is 240  $\mu$ s and the one with STP is about 100  $\mu$ s. The main switch with STP is switched off earlier than the one without STP, since  $v_o$  is predicted *a priori* before switching off the main switch. The output can revert to the steady state in two switching actions.

Fig. 7 shows the transient response when the output power is changed from 25 to 2 W. The converter is originally in continuous conduction mode at 25-W output and is changed into discontinuous conduction mode at 2-W output. The converter can revert to steady state in 600  $\mu$ s and two switching actions.



Fig. 9. Time-domain simulation results of the condition in Fig. 8.

TABLE II Comparisons of Transient Performance Indexes Shown in Figs. 8 and 9

ESR	Settling time(µs)	% output undershoot	% output overshoot	Max. inductor current (A)
0mΩ	112,7	8.41	0	14.80
20mΩ	102.4	8.39	0	14.70
40mΩ	86.8	9.11	0	14.68
60mΩ	78.8	10.57	0	14.40
80mΩ	74.1	12.83	0	13.90
100mΩ	70.5	15.66	0	13.33

Thus, the STP can effectively enhance the transient response of the buck converter using hysteresis control without significant modification in the control circuit. It can operate in both continuous and discontinuous conduction modes.

The ESR of the output capacitor is neglected in the above theoretical derivations. Several simulations had been carried out to study the effects of the ESR on the transient responses. Fig. 8 shows the state-plane trajectories when the ESR varies from 0  $\Omega$  to 100 m $\Omega$  in steps of 20 m $\Omega$ . Fig. 9 shows the time-domain simulation results. The initial condition of the simulations is that  $i_L = 0.1 \ A$  and  $v_o = 5 \ V$ . The output power is suddenly changed into the full load condition (50 W) (i.e.,  $i_L = 10 A$ ). Table II tabulates the transient performance indexes at different values of ESR. It can be observed that the percentage output undershoot increases and the settling time decreases, as the ESR increases. It is mainly because the ESR becomes a dissipative component in the circuit and damps the transient response. Thus, the transient period is shortened. Moreover, as shown in Fig. 9, due to the presence of the ESR, the output voltage will decrease abruptly during the transient.

Other simulations studying the change of the output power from full load (50 W) to half load (25 W) had also been carried out. The state-plane trajectories are shown in Fig. 10 and the time-domain simulation results are shown in Fig. 11. Table III tabulates the transient performance indexes. Again, the settling time is reduced, as the ESR is increased.



Fig. 10. State-plane trajectories of the converters when the converter is changed from full load to half load with the ESR of the output capacitor varying from 0  $\Omega$  to 100 m $\Omega$ .



Fig. 11. Time-domain simulation results of the condition in Fig. 10.

## IV. CONCLUSION

The STP technique that is applied to the hysteresis control has been proposed. It can enhance the transient response of the buck converter. The output voltage can revert to steady state within two switching actions when it is subject to large-signal disturbances. The STP performances have been verified with experimental measurements. Further research will be dedicated to

TABLE III Comparisons of the Transient Performance Indexes Shown in Figs. 10 and 11

ESR	Settling time(µs)	% output undershoot	% output overshoot	Max. inductor current (A)	
QmΩ	132.3	0	5.25	10	
20mΩ	122.6	0	5.23	10	
40mΩ	114.1	0	5.49	10	
60mΩ	106.9	0	6.04	10	
80mΩ	101.0	0	6.90	10	
100mΩ	96.1	0	8.09	10	

form a theoretical basis studying the sensitivities of the component values on affecting the performances and the operation in discontinuous conduction mode.

#### REFERENCES

- R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of dc-dc converters using feedforward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 1, pp. 181–192, Jul. 1986.
- [2] G. K. Schoneman and D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 25–35, Jan. 1989.
- [3] T. A. Froeschle, "Current-Mode Controlled Two-State Modulation," U.S. patent 4456 872, Jan. 26, 1984.
- [4] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. Applied Power Electronics Conf. Exp.*, Feb. 1998, pp. 170–176.
- [5] D. Goder and W. R. Pelletier, "V<sup>2</sup> architecture provides ultra-fast transient response in switch mode power supplies," in *Proc. High Frequency Power Conversion Conf.*, 1996, pp. 19–23.
- [6] S. Qu, "Modeling and design considerations of V<sup>2</sup> controlled buck regulator," in *Proc. IEEE Applied Power Electronics Conf. Exp.*, Mar. 2001, pp. 507–513.
- [7] R. Miftakhutdinov, "Analysis of synchronous buck converter with hysteretic controller at high slew-rate load current transients," in *Proc. High Frequency Power Conversion Conf.*, 1999, pp. 55–69.
- [8] P. T. Krein, *Elements of Power Electronics*, 1st ed. New York: Oxford Univ. Press, 1998.
- [9] W. W. Burns and T. G. Wilson, "State trajectories used to observe and control dc-to-dc converters," *IEEE Trans. Aerosp. Electron. Systs.*, vol. 12, no. 6, pp. 706–717, Nov. 1976.
- [10] —, "Analytical derivation and evaluation of a state trajectory control law for dc-to-dc converters," in *Proc. Power Electron. Spec. Conf.*, 1977, pp. 70–85.
- [11] S. D. Huffman, W. W. Burns, T. G. Wilson, and H. A. Owen, "Fast-response free-running dc-to-dc converter employing a state-trajectory control law," in *Proc. Power Electron. Spec. Conf.*, 1977, pp. 180–189.